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SEMICONDUCTOR APPARATUS

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SEMICONDUCTOR APPARATUS

FIELD OF THE DISCLOSURE

The present disclosure relates generally to semiconductor devices, and more particularly to thyristor devices and applications.

BACKGROUND

It is well known in the electronic arts that electrostatic discharge (ESD) can damage and/or destroy semiconductor devices. Protection circuitry is generally designed into semiconductor devices to reduce the risk of damage due to ESD. For example, thyristors are often used to reduce damage that can occur as a result of an ESD event on an input-output (I/O) of a semiconductor device. A circuit representation of a thyristor used as an I/O protection circuit is illustrated in FIG. 1.

The thyristor of FIG. 1 includes an anode node that is shorted through an n-type well tie (nwt) to the nwell, and a cathode node that is shorted through a p-type well tie (pwt) to the p-well. The thyristor of FIG. 1 is illustrated in cross-sectional view in FIG. 2, where the psd, and nsd notation indicate regions that can be formed using p-type and n-type source-drain formation processes respectively. Likewise, the n-well and p-well notations indicator regions that can be formed using well formation processes, while the pgc region is a doped region known to be used in various processes including Bipolar-Complimentary Oxide Semiconductor (BiCMOS) processes. The thyristor of FIG. 2 requires a voltage and trigger current large enough to protect against latch-up of the thyrister during normal operation, while still maintaining a trigger voltage sufficiently low to activate and clamp during an ESD event. However, the trigger voltage of the prior art thyrister of FIGs. 1 and 2 can result in too large a voltage drop when used in voltage sensitive applications, such as for providing ESD protection between in ground nodes.

Another technique to protect against ESD damage of semiconductor devices is to connect otherwise isolated ground references to each other using opposing p-n junction diodes in parallel. While this allows for ESD current to flow from one ground reference node to another, it does so

at the cost of introducing the diode junction capacitance between the two ground references, resulting in a reduced signal isolation between the grounds. The conventional thyristor of FIG. 1 if used to provide ESD protection between isolated ground nodes causes reduced signal isolation due to a relatively large associated capacitance of approximately 300 femptofarads, and has a trigger voltage which has been found to be too large to be an effective protection circuit against damage caused by ESD events. It should be apparent from the above discussion that a thyristor device capable of providing high conductance protection during ESD events and a high degree of signal isolation along with a low capacitance during normal operation would be useful.

BRIEF DESCRIPTION OF THE DRAWINGS

Various objects, advantages, features and characteristics of the present disclosure, as well as methods, operation and functions of related elements of structure, and the combination of parts and economies of manufacture, will become apparent upon consideration of the following description and claims with reference to the accompanying drawings, all of which form a part of this specification.

FIG. 1 illustrates a prior art thryristor circuit representation;

FIG. 2 illustrates a cross-sectional view of an implementation of the circuit of FIG. 1;

FIG. 3 illustrates in partial block diagram and partial circuit form a thyristor circuit representation in accordance with one embodiment of the present invention;

FIG. 4 illustrates in circuit form a thyristor circuit representation having a zener diode in accordance with one embodiment of the present invention;

FIG. 5 illustrates a cross-sectional view of an implementation of the circuit of FIG. 4;

FIG. 6 illustrates in partial block diagram and partial circuit form a thyristor circuit representation in accordance with one embodiment of the present invention;

FIG. 7 illustrates in circuit form a thyristor circuit representation having a field effect transistor in accordance with one embodiment of the present invention;

FIG. 8 illustrates a cross-sectional view of an implementation of the circuit of FIG. 47;

FIG. 9 illustrates in partial block diagram and partial circuit form a thyristor circuit representation in accordance with another embodiment of the present invention;

FIG. 10 illustrates in circuit form a thyristor circuit representation having a field effect transistor in accordance with another embodiment of the present invention; and

FIG. 11 illustrates a device using a thyristor to provide ESD protection to isolated voltage references.

DETAILED DESCRIPTION OF THE FIGURES

The present disclosure describes a low voltage thyristor and specific application embodiments implementing such a low voltage thyristor. The low voltage thyristor has a low voltage trigger to activate the thyristor at a voltage of approximately ten volts or less. This low voltage trigger allows for compensation of ESD (electrostatic discharge) events based on a human body model. Such a thyristor can be used to provide ESD protection between isolated voltage references, such as ground nodes, of data processing devices. Note that the term isolated voltage references indicates that in normal operation the voltage reference nodes are adapted to be isolated from each other, such that signal isolation is maintained between the voltage references. For example, isolated voltage references function such that normal operating noise on a first voltage reference node does not have a functional effect on devices connected to the second voltage reference node. FIGs. 3-12 illustrate specific embodiments in accordance with the present invention.

FIG. 3 illustrates a circuit representing a thyristor having a low voltage trigger 30. The low voltage trigger 30 is connected to the base of the PNP transistor 10 and to the base of the

NPN transistor 20. In operation, the low voltage trigger 30 activates the thyristor by drawing current from the base of the PNP transistor while simultaneously providing current to the base of the NPN transistor, thereby activating the thyristor by turning on both transistor 10 and transistor 20. A specific implementation of a low voltage trigger 30 is illustrated in FIG. 4.

FIG. 4 is analogous to FIG. 3 with a zener diode implementing the low voltage trigger 30. FIG. 5 further illustrates a cross-sectional view of the thyristor of FIG. 4. In the embodiment illustrated in FIG. 5, an anode connector 42 and a cathode connector 44 provide access to the thyristor structure which includes p-type region 51, n-type region 52, p-type region 53, and n-type region 54. Specifically, the anode connector 42 is connected to the p-type region 51, and the cathode connector 44 is connected to the n-type region 54. The various n-type and p-type regions represent regions of varying conductivity types (i.e. a p-conductivity type and an n-conductivity type). The boundary between immediately adjacent conductivity type regions are referred to as conductivity type junctions. For example, the p-n junction formed at the boundary between p-type region 51 and n-type region 52 is a conductivity type junction. Conductivity type junctions are formed in a similar manner between regions 52-53 and 53-54. It will be appreciated that the PNP transistor 10 of FIG. 3 is formed by the conductivity type junctions between regions 51-52 and regions 52-53. Likewise, NPN transistor 20 of FIG. 3 is formed by the conductivity type junctions between regions 52-53 and 53-54. The regions 61 and 62 of FIG. 5 implement the zener diode 60 of FIG. 4, as discussed in greater detail below.

During operation, the zener diode 60 will break down at a low voltage (i.e. the beginning of an ESD event) to allow current to flow from PNP 10 and provide current to the base of the NPN device 20. In one embodiment, the zener 60 is chosen to have a breakdown voltage of 10 volts or less, or approximately 10 volts or less. In another embodiment, the zener diode 60 is chosen to have a breakdown voltage of 6 volts or less, or approximately 6 volts or less. The term approximately is used to account for variations of various processing and operating variables that can prevent a precise parametric value, such as zener breakdown voltage, from being specified. For example, variations in processing are known to result in variations of parametric values, likewise operating temperatures can result in variations of specific parametric values, such as the

breakdown voltage of a zener diode. Because such variations are not entirely predictable the term approximately is used to qualify an expected value.

Referring again to FIG. 5, the zener diode is implemented by forming a p-type region 61 at least partially overlying region 53, and n-type region 62 overlying the p-type region 61 and the n-type region 52, such that the regions 61 and 62 at least partially overlie region 53. Note that region 61 FIG. 5 can also overlie a portion of region 52, even though it is not shown. It will be appreciated that the formation of the regions 61 and 62 to form zener diode 60 are know in the art. For example, the p-type region 61 can be formed using a channel implant processes such as those used with various BiCMOS processes. Likewise, the regions 51 and 54 can be formed using known p-type & n-type source-drain formation processes, respectively, while regions 52 and 53 can be formed using known n-type and p-type well formation processes, respectively. The anode nodes or connectors 42 & 44 include conductive traces 67 and conductive vias 65 formed within the interlevel dielectric layer 68.

FIG. 6 illustrates a circuit representing a thyristor having a low voltage trigger portion 32 coupled between the collector and the emitter of the NPN transistor 20. FIG. 7 illustrates a more specific circuit representing the thyristor of FIG. 6. Specifically, FIG. 7 illustrates an n-an n-channel field effect transistor (FET) 70 having its drain and gate commonly connected to the collector of the NPN transistor 20 and to the base PNP transistor 10. The source of the FET 70 is connected to the emitter of transistor 20. In this configuration, an ESD event on the anode will cause the FET transistor 70 to turn on, providing electrons to the base of the PNP transistor 10, resulting in the overall activation of the thyristor. A specific implementation of the device of FIG. 7 is illustrated in FIG. 8.

FIG. 8 illustrates a cross sectional view of a thyristor structure similar to the thyristor structure illustrated in FIG. 5. Analogous features between FIG. 8 and FIG. 5 are similarly numbered. The FET 70 is represented in FIG. 8 by n-type region 71 (drain current node), gate structure, n-type region 54 (source current node), and conductive portion 73. Note conductive portion 73 is illustrated to include vias and a metal trace, to connect the gate structure 72 to n-type region 71. The n-type region 71 is electrically coupled to n-type region 52 so that an ESD event on the anode causing current to flow into the region 52 will result in the gate 72 voltage to

rise creating an n-channel in the underlying substrate, thus resulting in current to flow from the base of the p-type transistor (region 52) causing the thyristor to turn on.

FIG. 9 illustrates a thyristor having a low voltage trigger connected to the collector of transistor 20, the emitter of transistor 20, and to the anode. FIG. 10 illustrates a specific implementation the thyristor of FIG. 9. Specifically, FIG. 10 illustrates a circuit representing a thyristor using a FET 80 in a manner similar to that described with reference to FIGs. 7 & 8. However, the gate of the FET 80 of FIG. 10 is connected to the anode instead of its own drain. The thyristor implementation of FIG. 10 can be used in a specific embodiment when the anode and cathode are connected to common reference nodes, whereby an ESD event will result in the FET 80 turning on to drawn current from the base of PNP transistor 20, thereby triggering the thyristor.

One advantage of the devices described with reference to FIGs. 8 and 10 is that they can be readily implemented using CMOS (complimentary metal oxide semiconductor) processes, as opposed to more costly processes, such as BiCMOS processes.

FIG. 11 illustrates a device 100 having a plurality of circuit portions, including circuits 110 and 120. The device 100 will generally be an integrated data processing device, such as a microprocessor, microcontroller, or other system on a chip applications. Circuits 110 and 120 are respectively connected to ground nodes GND1 and GND2, which are connected to each other internally by an ESD protection circuit that includes thyristors 115 and 120 of the type described herein. Generally, one of circuit 110 and 120 will be more sensitive to noise on a voltage reference node, such as a ground node, that the other circuit. Examples of specific circuits that can be sensitive to noise include analog circuits, including radio frequency analog circuits. Therefore, isolation techniques are often used to accommodate the need for a low noise reference source by sensitive circuitry. However, in the event of an ESD event on one of the reference sources, it is desirable to allow for a current path to the other reference source to help dissipate any potentially damaging current from such an event. By using low voltage thyristors 110 and 120, which are of the type described herein, a low capacitance connection, that provides high conductivity at a low trigger voltage is realized.

FIG. 12 illustrates a flow diagram of a method in accordance with the present invention. At step 201, a voltage difference is detected between two voltage reference nodes in order to detect an ESD event. The voltage reference nodes will generally be at the same voltage potential during normal operation. However, it would be anticipated that voltage reference nodes can be at different potentials during normal operation, provided step 201 takes into account the normal voltage difference.

At step 202, a conductive path is provided between the two voltage reference nodes in order to shunt the ESD event current from one voltage reference node to the other, thereby providing protection against an ESD event.

In the preceding detailed description of the figures, reference has been made to the accompanying drawings which form a part thereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical, and/or electrical changes may be made without departing from the spirit or scope of the invention. For example, while the specific examples have been illustrated as protecting against ESD events that may occur on one of a plurality of ground nodes, it will be appreciated that the techniques described apply equally as well to reference nodes having a common voltage. In addition, it will be appreciated that many other varied embodiments that incorporate the teachings of the invention may be easily constructed by those skilled in the art. Accordingly, the present disclosure is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention. The preceding detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present disclosure is defined only by the appended claims.